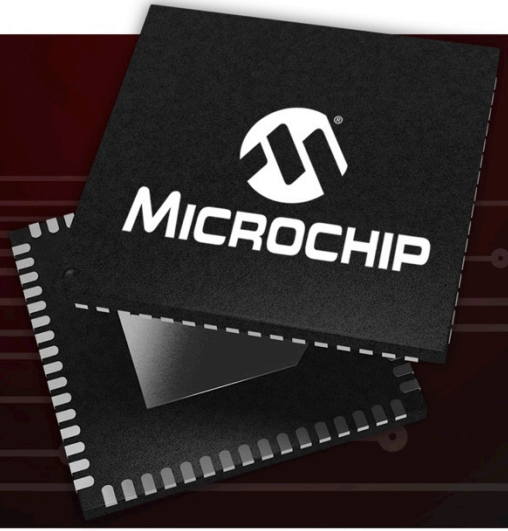
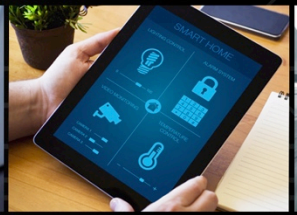
MICROCHIP



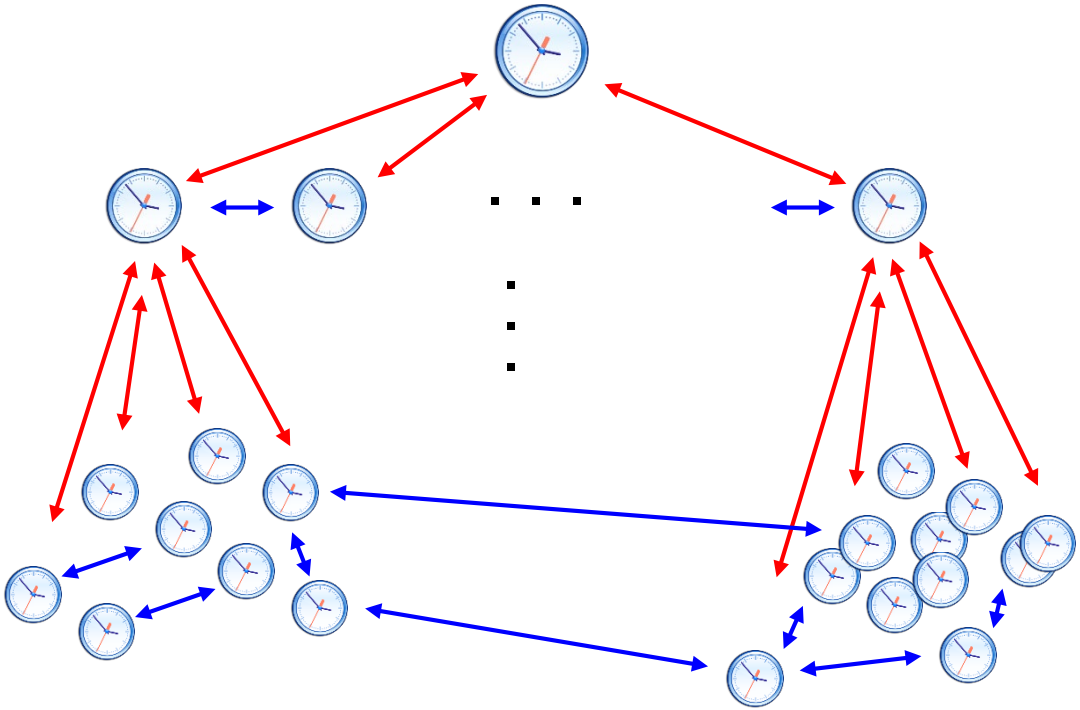
A Leading Provider of Smart, Connected and Secure Embedded Control Solutions






Tactical Atomic Clocks
Robert Lutwak
22 October 2019

Timing Networks



https://upload.wikimedia.org/wikipedia/commons/thumb/8/8f/Crystal_Clear_app_clock.svg/240px-Crystal_Clear_app_clock.svg.png

Timing Networks

- **Point-of-use timing performance is determined by:**
  - Quality and availability of time-transfer links
  - Quality and performance of local oscillator (LO, i.e. clock)
- **With robust and reliable GPS availability:**
  - Link instability (Allan deviation) of $\sigma_y(\tau) \cong 10^{-8}/\tau$
  - Demands on LO are modest
- **In GPS-degraded and -denied environments:**
  - Link instability is variable, and connection is sporadic
  - Requires superior LO to integrate between synchronization events

Better Clocks are Better

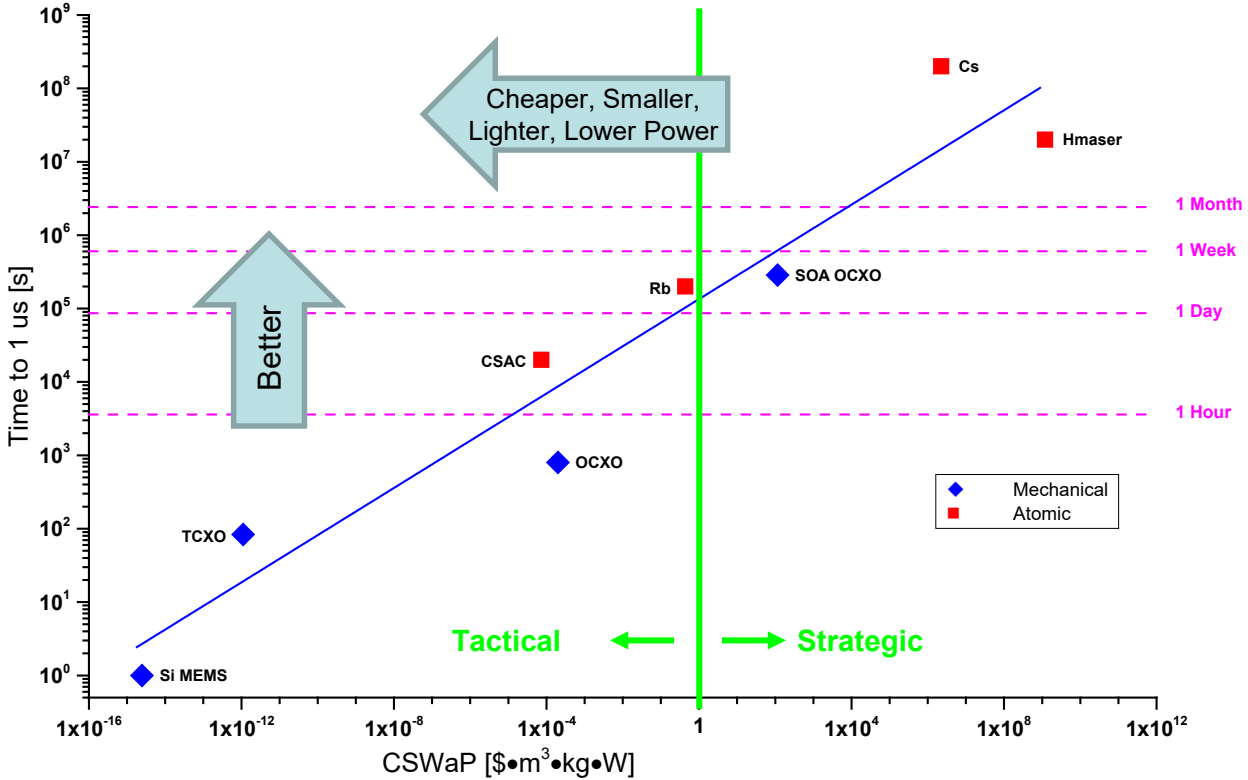
- **Improved stability for integrating synchronization**
- **Flywheel to provide timing when link is down**
- **When combined with GPS:**
  - Improved phase noise and short-term stability
  - Navigation with fewer than four satellites
  - Anti-spoof and anti-jam protection
  - Direct P(Y) and M-code acquisition
  - Improved vertical dilution of precision (VDOP)

Continuous Improvement

- **As the timing battlespace becomes increasingly contested…**
  - Need robust, fault-tolerant timing networks
  - Require alternative links for synchronization
  - Require improved clock performance at all levels of cost, size, weight and power (CSWaP)

- **I'm going to talk about clocks…**

Available Clocks



ΔT=5°C

Available Atomic Clocks

Hydrogen Maser
≈ $250K
≈ 100 W
σ_y(1 sec) ≈ 2 x 10^{-13}
Drift ≈10^{-16}/day

Chip-Scale Atomic Clock (CSAC)
≈ $2K
≈ 100 mW
σ_y(1 sec) ≈ 10^{-10}
Drift ≈ 10^{-11}/day

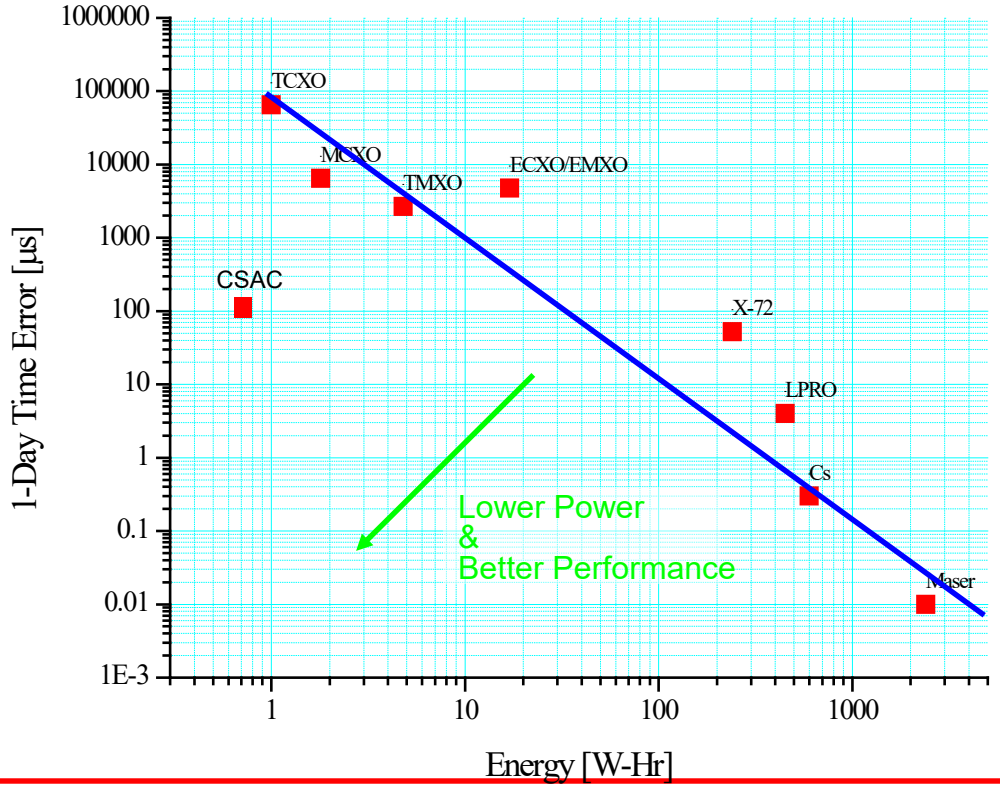
Rubidium Oscillator
≈ $2K
≈ 10 W
σ_y(1 sec) ≈ 10^{-11}
Drift ≈ 10^{-12}/day

Cesium Beam Frequency Standard
≈ $75K
≈ 30 W
σ_y(1 sec) ≈ 10^{-11}
Drift ≈ 0

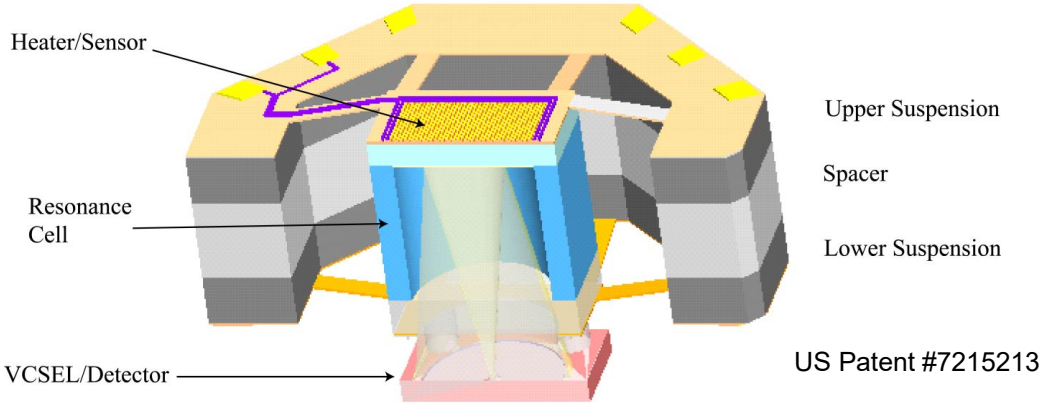
A Bit of History…

- **1990-2000: DARPA Miniature Time Standard Program**
- **2000-2010: DARPA CSAC Program**
- **2010-2012: US Army ManTech CSAC Program**
- **2011: Symmetricom SA.45s product release**
- **Today:**
  - Microchip has shipped over 100,000 CSACs
  - DoD systems and applications are emerging
  - US and international competitive development continues apace

The CSAC Challenge



SA.45s Physics Package

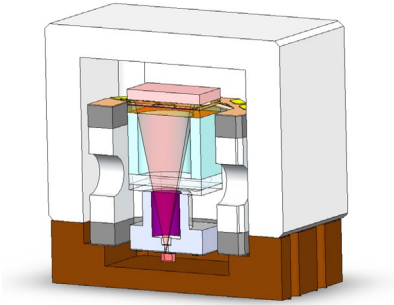


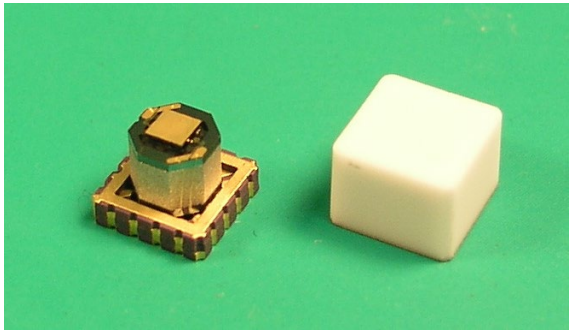
US Patent #7215213

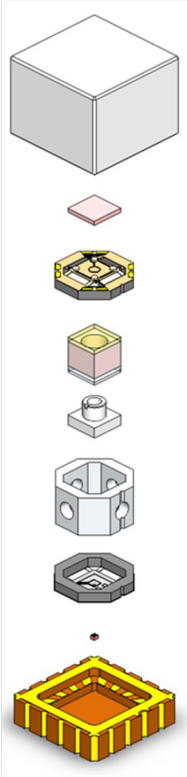
- Suspension design based on tensioned polyimide
  - High strength (withstands >2,000 g loads)
  - Low vibration sensitivity (Resonant frequency above 2 kHz)
  - Low-thermal conductivity (7000 °C/Watt)
  - Provides support for minimal electrical traces
- VCSEL operates at resonance cell temperature
  - Essential for CSAC deployment in real-world applications
  - CSAC can run at 70°C ambient with 85°C cell temperature

M. Mescher, et. Al., "An Ultra-Low-Power Physics Package for a Chip-Scale Atomic Clock," *Proceedings of the 13th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers '05)*, Seoul, Korea, June 5-9, 2005, pp. 311-316.

SA.45s Physics Package





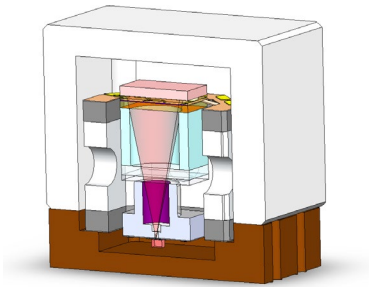


CSAC Priorities

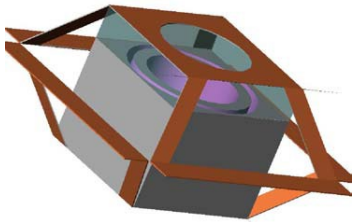
1. Sell Price
2. TempCo
3. Aging
4. Retrace
5. Power Consumption
6. Size
7. Short-Term Stability

CSAC Status

- **Highly competent manufacturing/materials team has come a long way**
  - Yields continue to improve month-over-month
  - Most failures are traced to root cause - usually workmanship or vendor part quality
  - Continuous process improvement and minor product modifications are driving down cost
- **Understanding of physics and performance trade space is well understood**
  - Data on over 100,000 CSACs
- **Microchip continues to invest IRaD in product improvement:**
  - Yield improvement
  - TempCo and aging improvement
  - Power reduction
  - Cost reduction



Today



From Datum CSAC Proposal to DARPA, circa 2000

CSAC Path Forward: CSAC 2.0

- **Limits of SA.45s technology (Robert's opinion):**
  - TempCo: <5e-11 over -40C to +85C
  - Aging: <5e-11/month
  - Sell price: $1000
- **Existing SA.45s is largely similar to DARPA proof-of-concept, circa 2000**
  - Answer "Is CSAC possible?" (spoiler alert: yes)

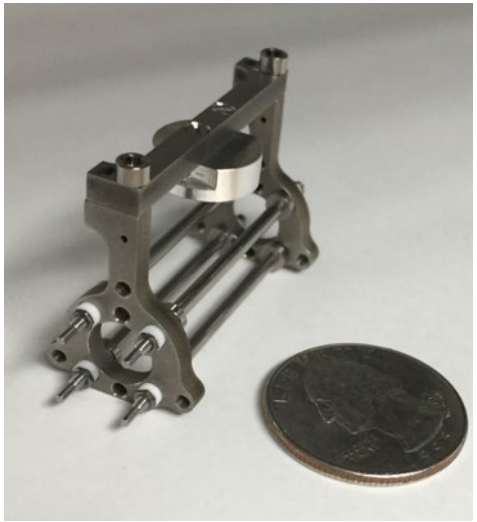
- **Opportunity:**
  - Leverage evolved understanding of CSAC physics
  - Leverage advances in MEMS, photonics and atomic physics
  - Start over with a clean whiteboard
  - Target improved manufacturability, reduced cost, improved performance
  - CSAC 2.0 should develop a truly ***chip-scale*** atomic clock

Architecture Limitations

- **SA.45s architecture has fundamental performance limitations**
  - Collision-shift of frequency due to collisions (Cs-Cs, Cs-wall, Cs-buffergas)
  - AC Stark shift of frequency (“light shift”) due to continuous laser illumination
- **Future much-higher-performance CSACs require new architectures**
  - DARPA IMPACT Program (2008-2013)
  - DARPA ACES Program (2015-Present)
  - Candidate technologies:
    - Laser-cooled “drip” clocks ← Shock/vibration challenged
    - Optical carrier clocks ← Long path to robust low-CSWaP optical frequency synthesis
    - Trapped-ion clocks ← Robust to vibration and *relatively* straightforward

Ion Clocks

- **Ideal for tactical applications:**
  - Trapped ions are isolated from environment
  - Shock and vibration immune
  - Potentially low-CSWaP
- **Ion clock research goes back 30 years:**
  - mercury (Hg+), cadmium (Cd+), ytterbium (Yb+), …



Compact Yb+ trap

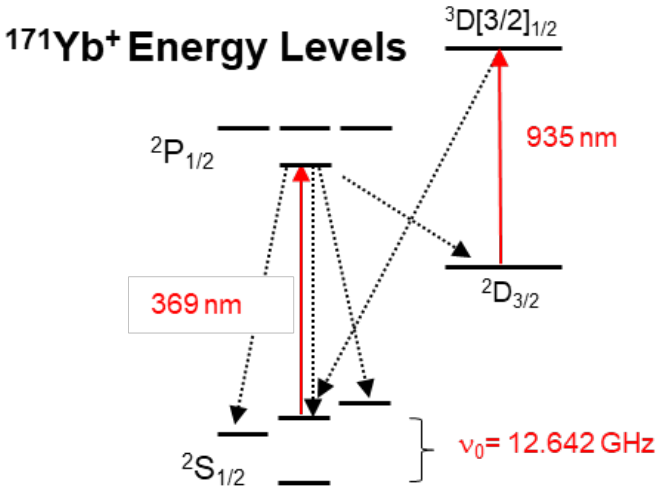
from *Tallant, et. al., IEEE FCS 2019*

Ytterbium Ion Clocks

- **Why Yb^+ ?**
  - 12.5 GHz hyperfine frequency
    - Low-power microwave synthesis in silicon CMOS
  - 369 nm laser for optical pumping/interrogation
    - High signal rate eases burden on LO vs. lamp pumping (e.g. Hg^+)
    - Available cycling transition for laser cooling (high performance)
- **Yb^+ is scalable:**
  - Higher-performing battery-powered CSAC
  - Compact tactical clock
  - Laser-cooled high-performance clock
  - Optical carrier clock

Yb+ Energy Structure

- **Yb^+ requires microwaves + two lasers:**
  - Clock interrogation at 12.6 GHz (easy)
  - **Signal at 369 nm** (challenging)
  - Repumping at 935 nm (easy)
- **Ion trap technology is mature**
  - Used extensively by the mass spectrometer community
  - Minimal complexity vs. trapped neutrals
- **369 nm laser is primary challenge**
  - Extended-cavity Fabry-Perot diode lasers are available for lab use but extremely vibration sensitive.
  - Distributed Bragg Reflectors (DBR) could be developed by extension of Fabry-Perot Lasers



369 nm Laser for Yb+

- **Need “spectroscopic grade” laser:**
  - Narrow linewidth:
    - < 100 MHz for buffer-gas-cooled Yb+ clock
    - ≈ 1 MHz for laser-cooled clock
  - Single mode (longitudinal, transverse, polarization)
  - No mode-hops
- **Edge emitters at 369 nm already exist**
  - Epitaxial growth and gain are solved problems
  - 369 nm is on the edge of accessible semiconductor laser wavelengths in GaN
  - DBR device is a relatively straightforward development
- **Lowest CSWaP requires vertical-cavity surface emitting laser (VCSEL)**
  - Challenging development due to GaN material and processes

369 nm is not Just for Clocks

- **Yb^+ clocks are a Quantum Information System (QIS) technology pathfinder**
  - Yb^+ is used extensively by the Quantum Information community for the same reasons that it is attractive as a clock
  - Laser requirements are similar
  - QIS isn't concerned with CSWaP yet…but they will be eventually
- **Clocks are an immediate need with ready applications**
- **369 nm laser development will lay the groundwork for future QIS**

Thank You

Robert.Lutwak@Microchip.com